Integrated Neurotechnologies Laboratory

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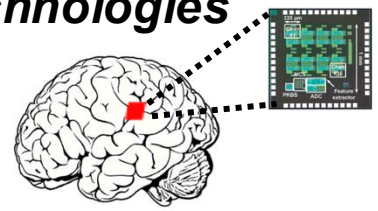


Advanced analog integrated circuit design (EE-523), Lecture 7

Armin Tajalli (invited speaker, visiting Professor)

Institutes of Electrical and Micro Engineering and Neuro-X, School of Engineering, EPFL

Advanced Analog Integrated Circuit Design (EE-523), Lecture 7

Sigma-Delta ADC

Prof. Armin Tajalli, University of Utah

Spring 2025

Outlines

- Basic Concept
- Background
- Oversampling Process
- Noise shaping
- Implementation
- Non-ideal effects
- More complex topologies
- Summary

Basics of Sigma-Delta ADCs

Introduction
Overall Specifications

- SD architecture offers a very high level of precision (12 to 24 bits)
- Key concept: oversampling and noise shaping
- Slower than SAR and pipeline ADCs, but offers higher resolution
- Resolution range: 13 to 24b
- Frequency range: kS/s to MS/s

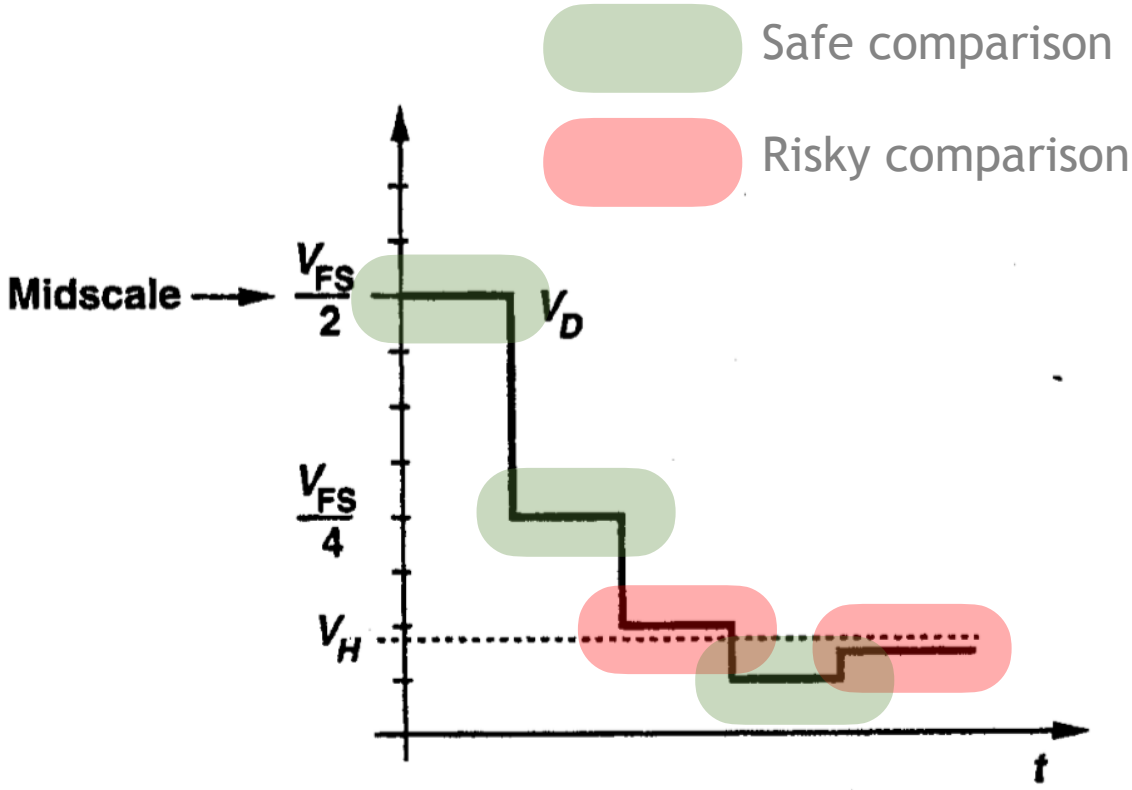
Background

Background
Challenges to Improve Resolution

- There is a growing demand for implementing high-resolution data converters.
- Traditionally, audio systems require 16b or more resolution for providing a proper sound quality.
- Internet-of-Thing (IoT) is a new field, where high resolution data converters are essential (high-precision sensor interface).

Background
Challenges to Improve Resolution

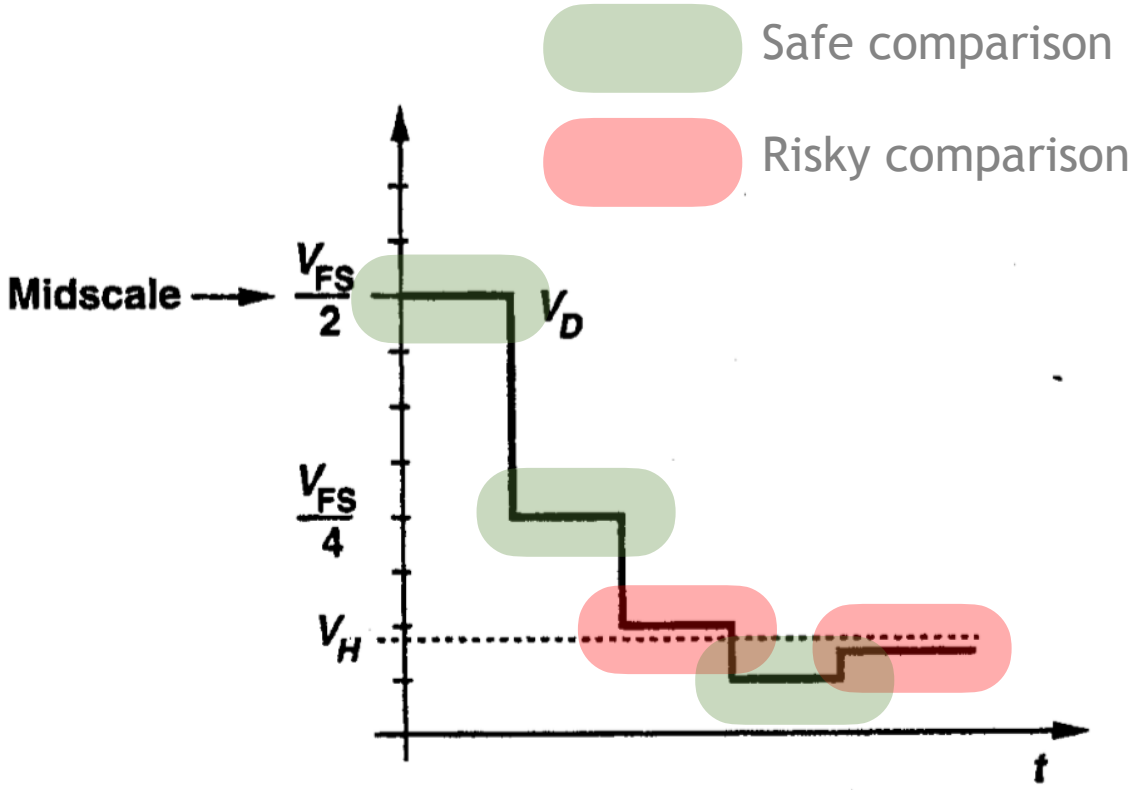
- SAR ADCs are energy-efficient and fast, however their resolution can not be extended beyond 12b
- There are some reports where resolution is above 12b, however employ heavy calibrations.
- What indeed is limiting the resolution of SAR ADCs?



Background
Challenges to Improve Resolution

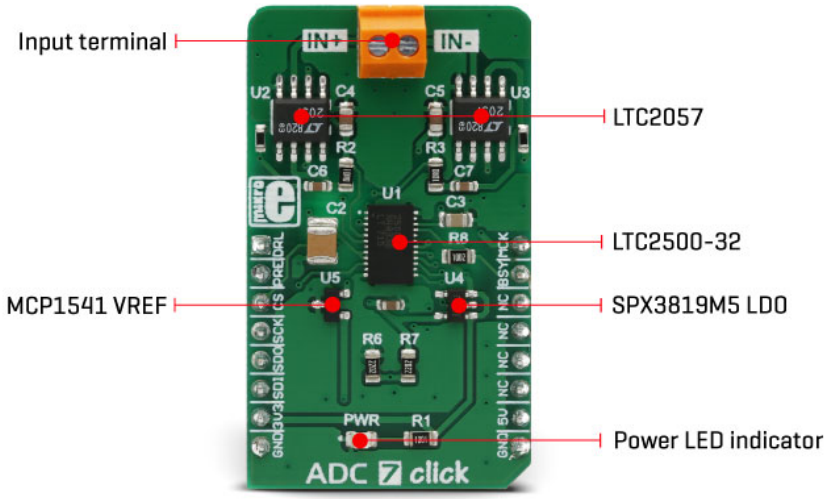
- There are at least two comparisons during the SAR process that suffer from noise and also device mismatch.
- SAR does not employ any correction mechanism to mitigate these issues (noise and device and mismatch).
- The other issue, that cannot be addressed easily, is meta-stability.

- Conclusion: resolution of SAR will be limited to ~ 12b.



Background
Challenges to Improve Resolution

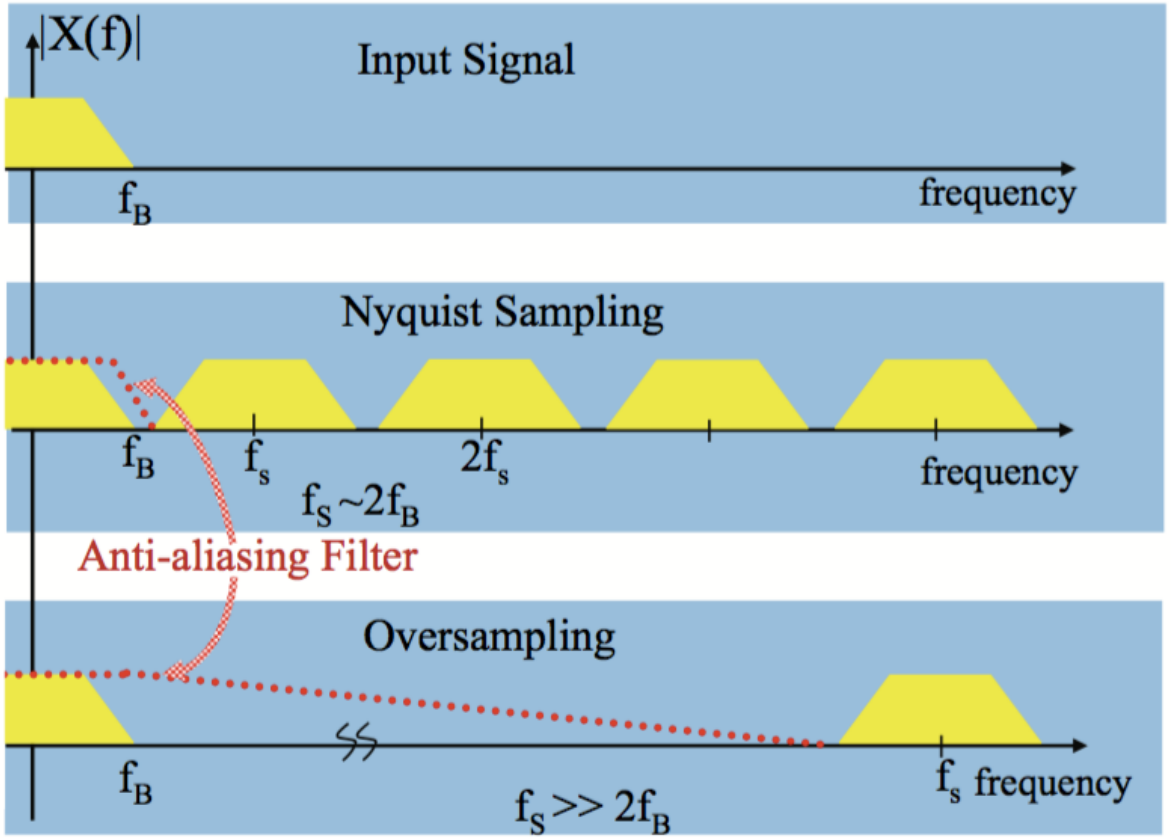
- Having said that, there are examples of oversampled-SAR, where resolution is high.
- Example: oversampled-SAR with 32b resolution, operating at 61 Samples per second.



Oversampling Process

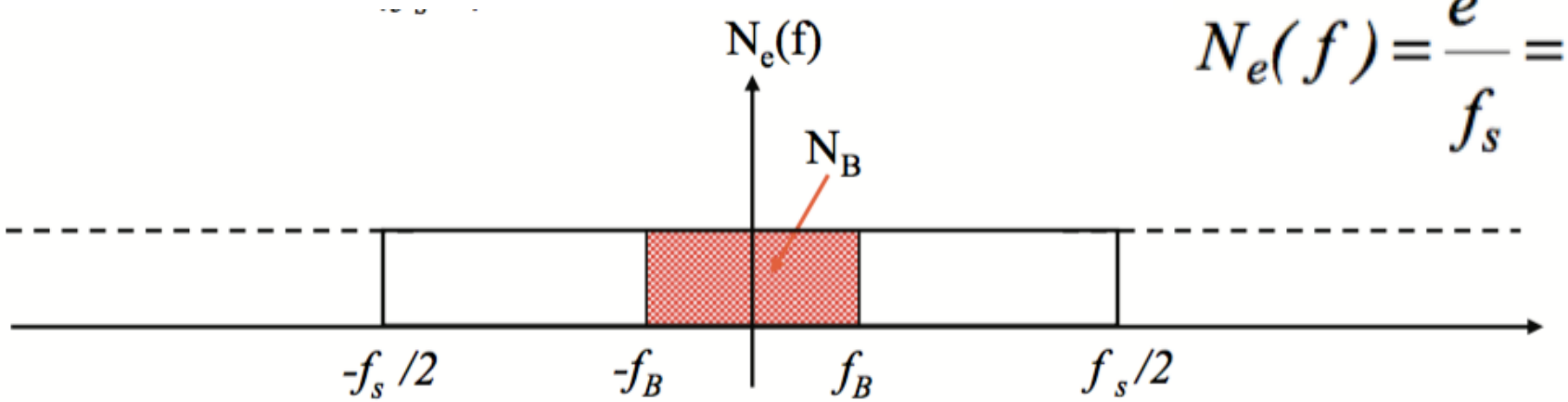
Introduction
Oversampling Concept

- Main goal: do some extra signal processing in order to improve precision of data converters.
- Concept: could we use averaging to improve precision ?
- Example, take few extra samples, consider the average value of those samples, thus remove random and quantization noise.



Introduction
Oversampling Concept

- Key Concept: reduce the effective quantization noise with reducing the integration BW:
  - Quantization noise power is indeed inversely proportional to the sampling frequency.



$$N_e(f) = \frac{\overline{e^2}}{f_s} = \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}$$

Introduction
Oversampling Concept

- Integrating the noise over a smaller BW, results in lower RMS quantization noise.
- Note: to reduce the noise power using averaging technique, the noise source needs to be random.

$$S_B = \int_{-f_B}^{f_B} N_e(f)df = \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}df$$

$$= \frac{\Delta^2}{12}\left(\frac{2f_B}{f_s}\right)$$

Introduction
Oversampling Concept

- Equivalently, SNR of ADC can be improved by increasing the number of samples per unit interval:
  - Increase the oversampling ratio (OSR) to enhance SNR.
- Example: Multiplying OSR by four, results in one bit more resolution

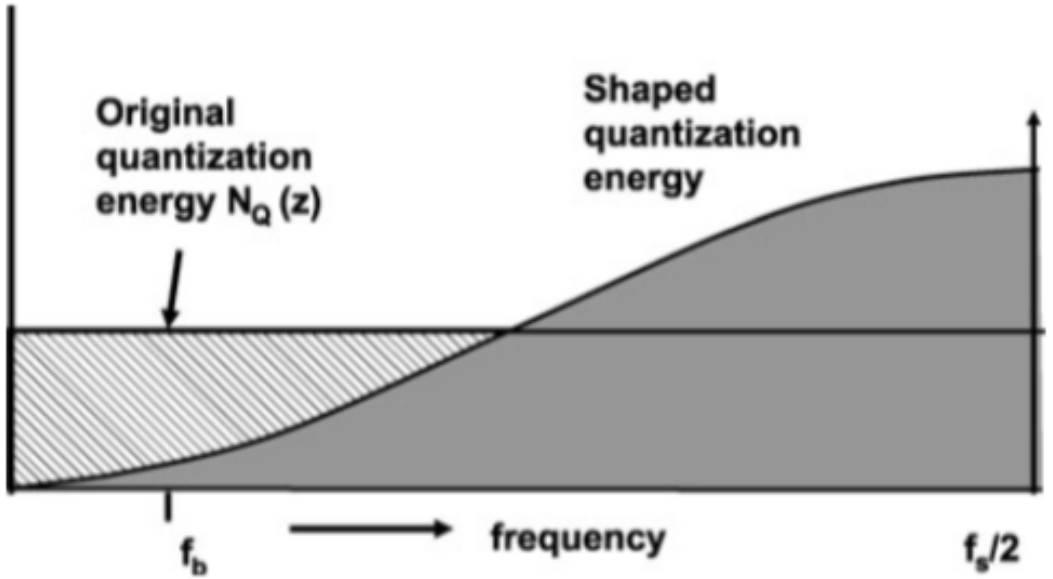
$$\mathrm{OSR} = \frac{f_s}{f_{s,ny}} = \frac{f_s}{2f_b}$$

$$Q_b^2 = \frac{V_{\mathrm{LSB}}^2 f_b}{6f_s} = \frac{V_{\mathrm{LSB}}^2}{12}\frac{1}{\mathrm{OSR}}$$

Noise Shaping

Introduction
Noise Shaping

- Main goal: filter out quantization noise by proper choice of the system Noise Transfer Function (NTF).
- High-pass filters can push out the quantisation noise from the band of interest.

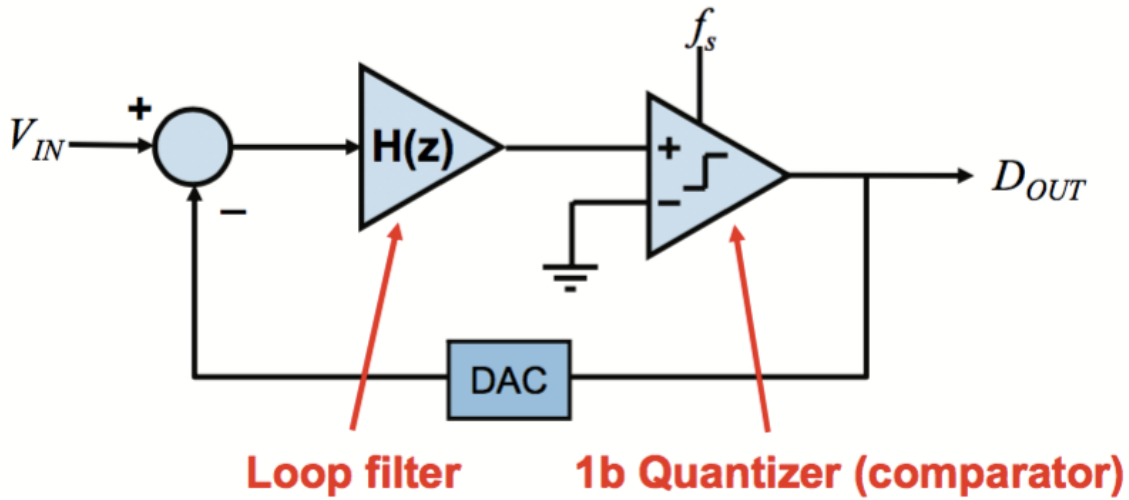


Introduction
Noise Shaping

- **Fundamental Concept:** Use a feedback structure, in which the Signal Transfer Function (STF) is low pass, while the NTF is high-pass.

- **Example:** A first order SDM
  - SDM: Sigma-Delta Modulator
  - H(z): an integrator or a low-pass filter.

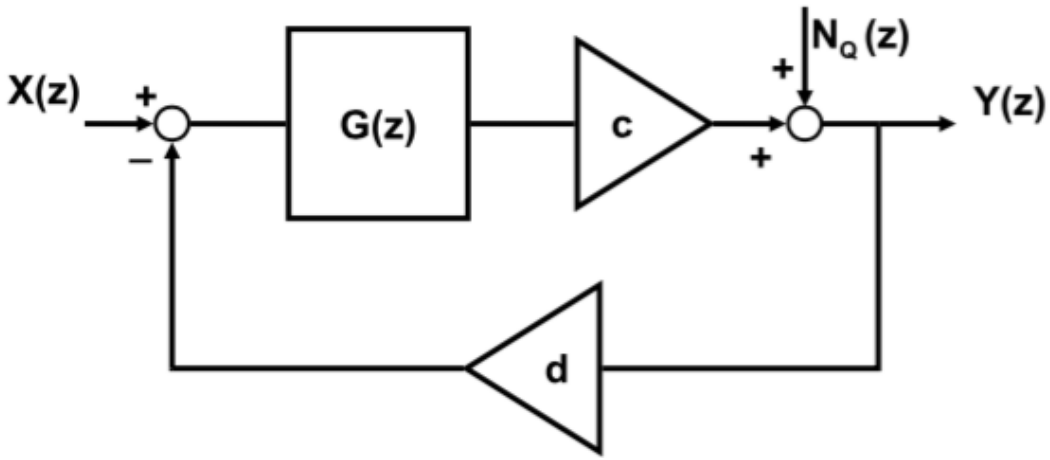
- **Question:** any similarity to the SAR architecture?



Introduction
Noise Shaping: Analysis

- Small signal model of a first order SDM is shown:
  - G(z): integrator
  - NQ: low-resolution ADC. For example, this low-resolution ADC can be a single bit converter.
  - Quantization noise is modeled at the output of the comparator (or: 1b /ADC)

$$Y(z) = X(z) + [1 - z^{-1}]N_Q(z)$$



Introduction
Noise Shaping: Analysis

- The z^{-1} operator represents a unit delay in time domain.
- The unit delay can be represented in frequency domain (Laplace Transform):

$$Y(z) = X(z) + [1 - z^{-1}]N_Q(z)$$

$$z = e^{j\omega T_s}$$

Introduction
Noise Shaping: Analysis

- Frequency domain transfer function can be estimated using z-domain formulation.
- The noise transfer function is high-pass, while the signal transfer function is low pass.

$$Y(z) = X(z) + [1 - z^{-1}]N_Q(z)$$

$$Y(\omega) = X(\omega) + (1 - e^{-j\omega T_s})N_Q(\omega)$$

$$|\mathrm{NTF}(\omega)|^2 = \left|\frac{Y(\omega)}{N_Q(\omega)}\right|^2 = |1 - e^{-j\omega T_s}|^2 = 2 - 2\cos(\omega T_s)$$

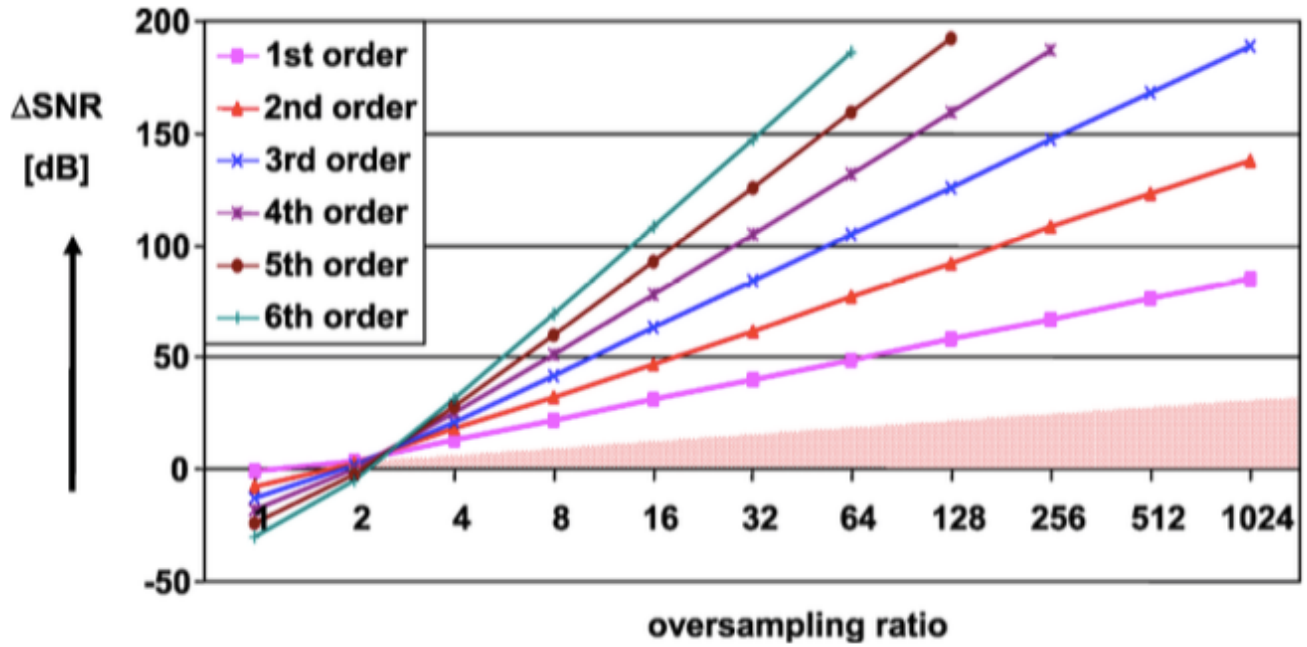
Introduction
Noise Shaping: Analysis

- Noise shaping helps to improve the achievable SNR furthermore.
- Noise power can be calculated by:

$$\frac{V_{LSB}^2}{12}\frac{\pi^2}{3OSR^3}$$

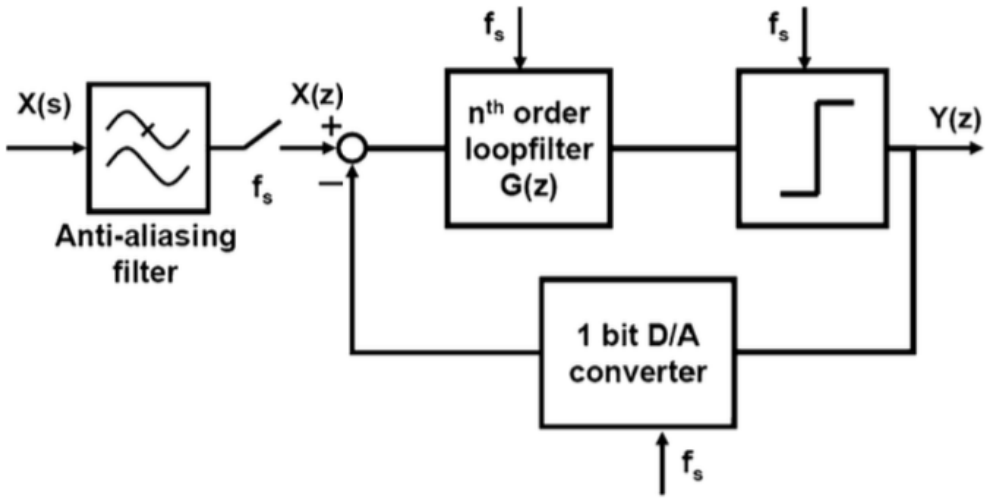
Introduction
Noise Shaping

- Higher order noise shaping can be achieved using higher order filters.



Introduction
Noise Shaping

- Further noise shaping using higher-order filter in the loop.
- This example shows a single-loop including a high-order filter
- The resolution of ADC used inside the loop can be as low as 1b.



$$Y(\omega) = X(\omega) + (1 - e^{-j\omega T_s})^n Q(\omega)$$

$$\left(\frac{V_{LSB}^2}{12}\right) \times \left(\frac{1}{OSR}\right) \times \left(\frac{\pi^{2n}}{(2n+1)OSR^{2n}}\right)$$

Overall Quantization Noise of a SDM

Quantization Noise of the in-loop ADC

$$\left(\frac{V_{LSB}^2}{12}\right) \times \left(\frac{1}{OSR}\right) \times \left(\frac{\pi^{2n}}{(2n+1)OSR^{2n}}\right)$$

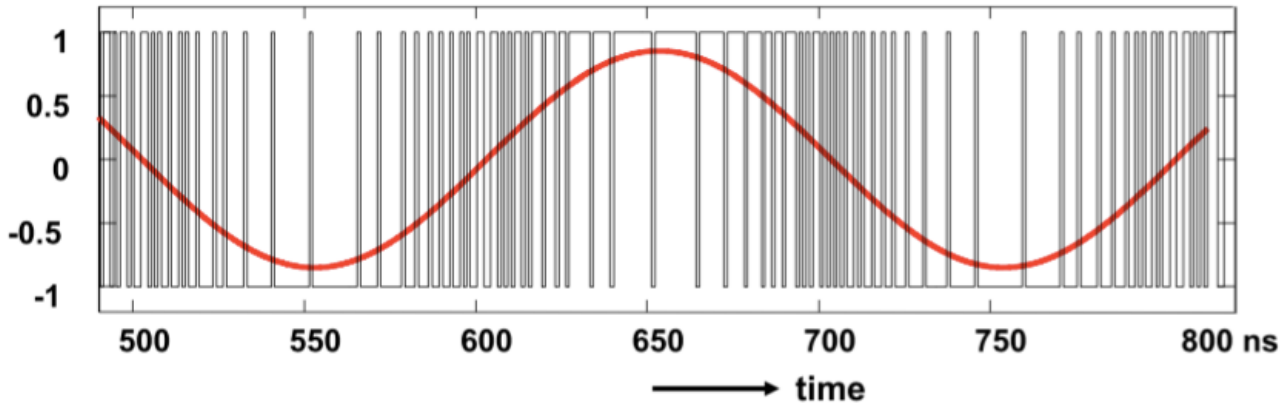
Quantization Noise improvement due to OSR

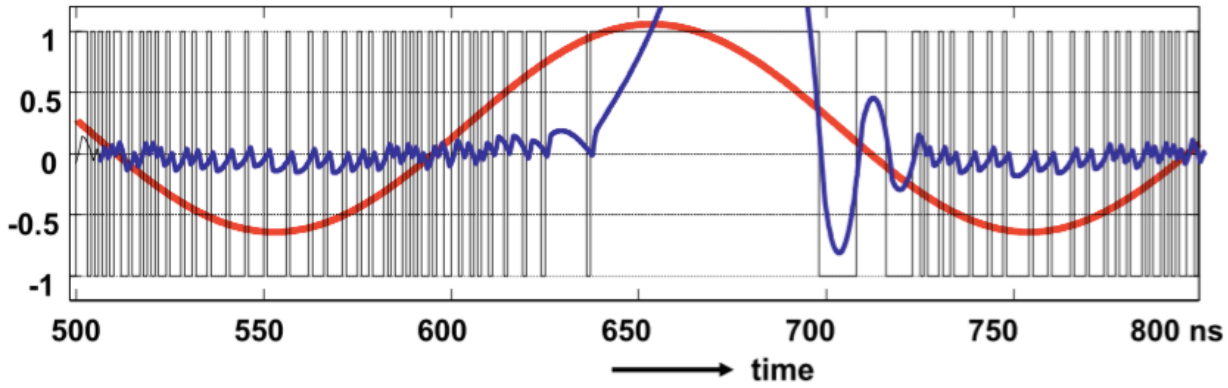
Quantization Noise filtering effect thanks to SDM

Introduction
Noise Shaping

- Time domain waveform:
  - Top plot shows the output of a SDM system.
  - Red: input sine wave
  - Gray: output of SDM

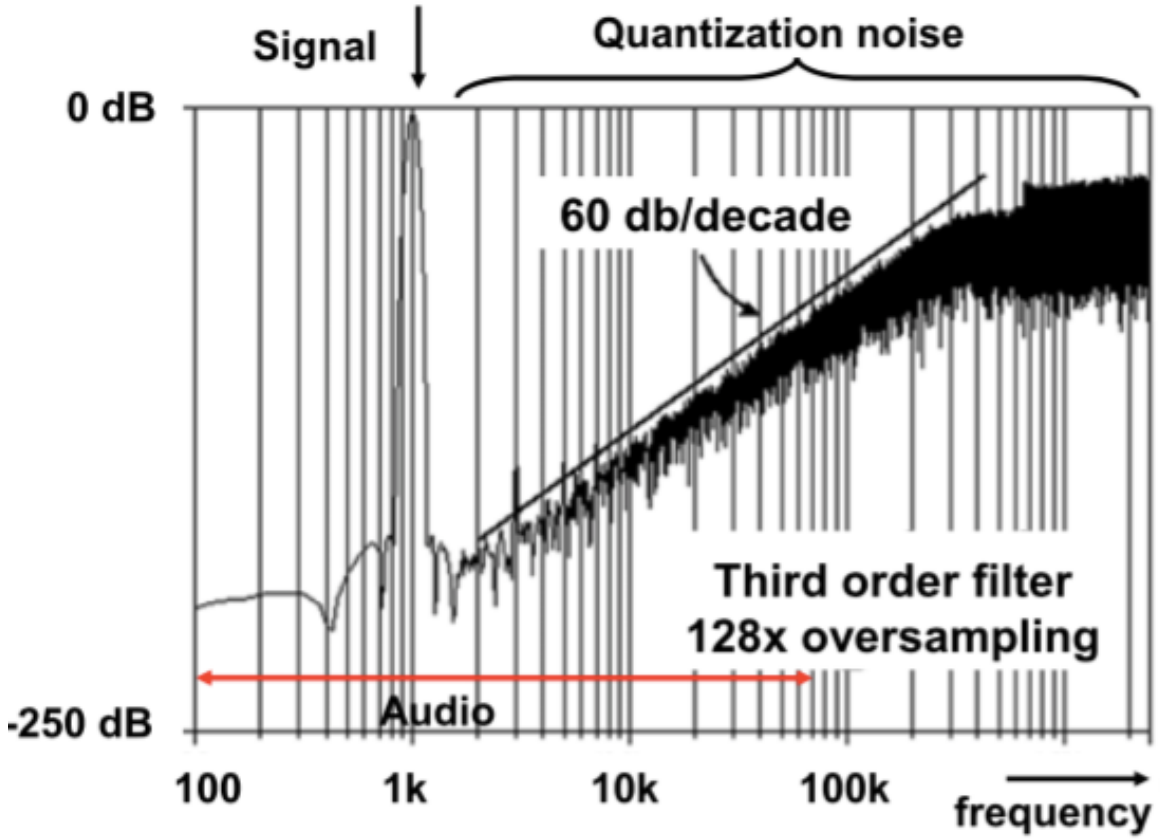
- When the input signal is out of the expected signal range, it causes instability, saturation.
  - Also it takes a bit of time to comeback to the normal mode of operation





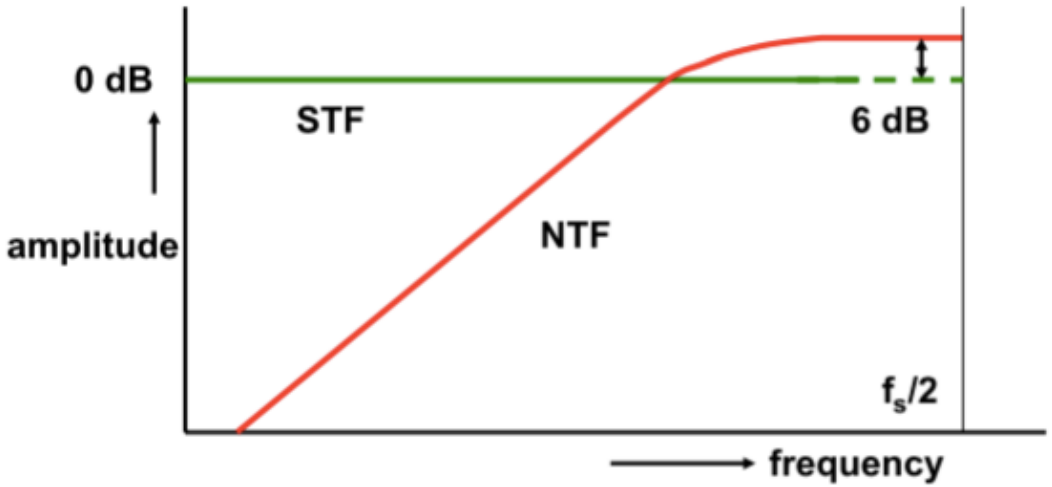
Introduction
Noise Shaping

- Example: a 3rd order filter has been used to enhance the noise filtering.
  - Signal is at 1 kHz
  - Noise shaping shows a third order transfer function (60 dB/dec).
  - Oversampling ratio (OSR) = 128



Introduction
Noise Shaping

- In a SDM structure, the NTF and the STF are different (noise and signal transfer functions):
  - STF is preferably an all-pass signal
  - NTF generally has a high pass transfer function.



$$Y(\omega) = \mathrm{STF}(\omega)X(\omega) + \mathrm{NTF}(\omega)N_Q(\omega)$$

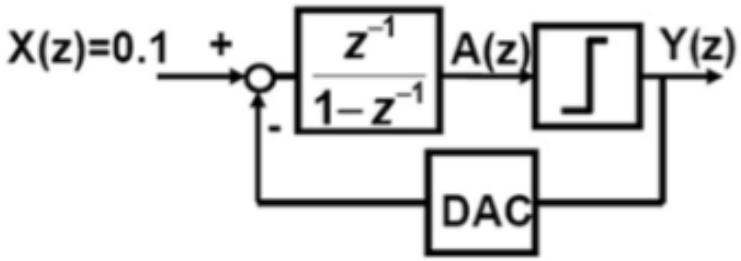
$$\mathrm{STF}(\omega) = \frac{cG(\omega)}{1 + cG(\omega)}$$

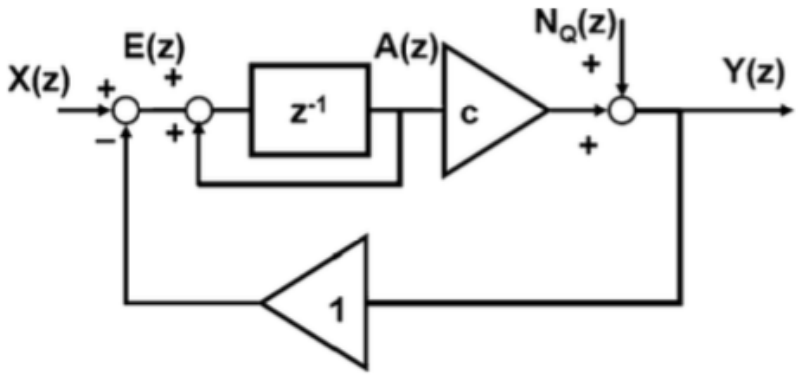
$$\mathrm{NTF}(\omega) = \frac{1}{1 + cG(\omega)}$$

Implementation

Implementation Switched-Cap Filter

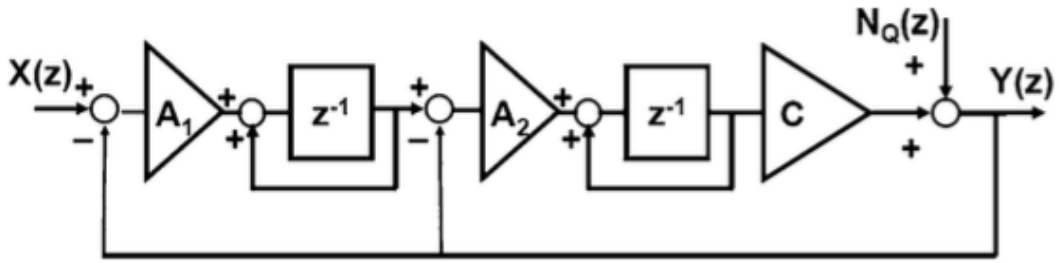
- SDM order: 1st order
- Type of filter: discrete-time (e.g., switched cap)
- Resolution of loop ADC: 1b
- Integrator transfer function:
  - $H(z) = 1+z^{-1} = z^{-1}/(1-z^{-1})$
  - Sum up every input with the previous value (integrator)





Implementation Switched-Cap Filter

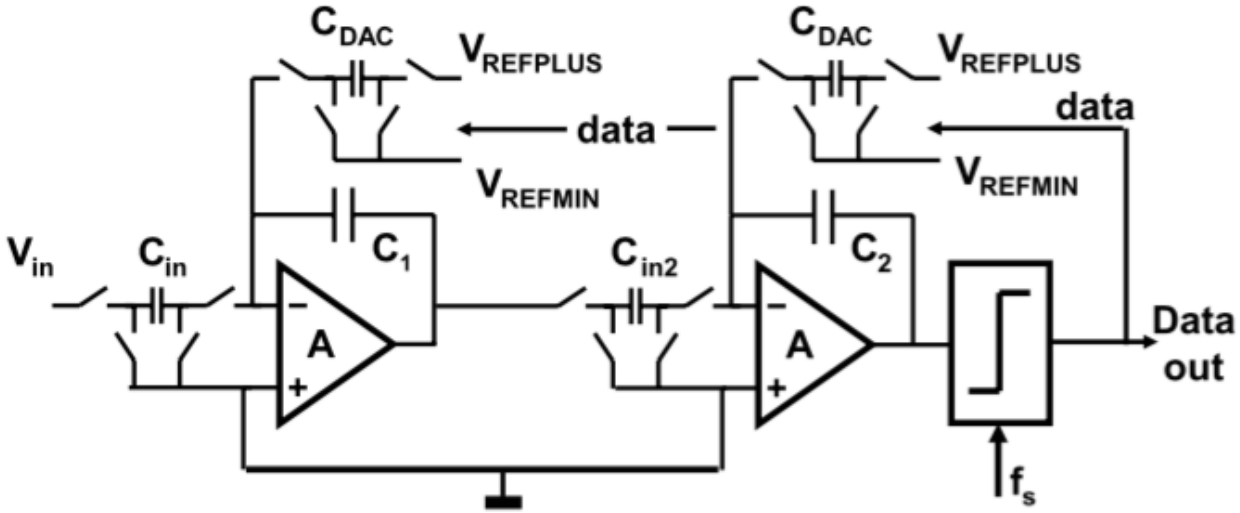
- SDM order: 2nd
  - STF = z^{-1} (an all-pass filter, with one unit delay).
  - NTF = $(1-z^{-1})$, which is a differentiator, or high-pass filter.



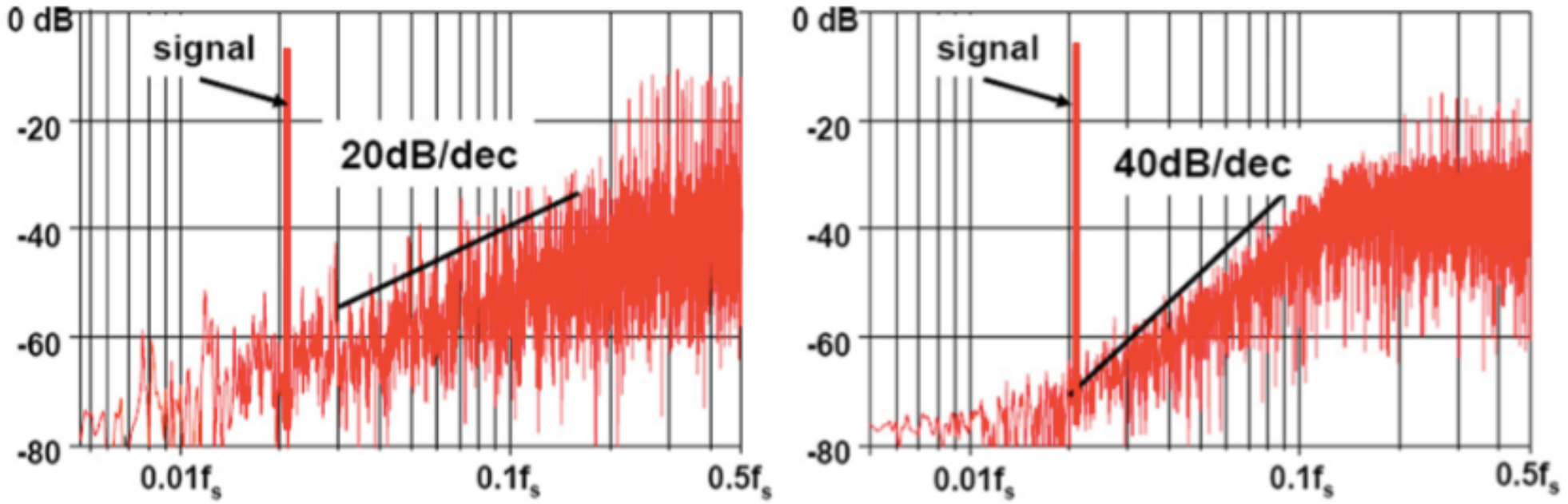
$$Y(z) = \underbrace{z^{-1}}_{\text{LPF}} X(z) + \underbrace{\left(1-z^{-1}\right)^2}_{\text{HPF}} E(z)$$

Implementation Switched-Cap Filter

- Single-ended circuit diagram of a switched-cap SDM:
  - Generally a differential circuits are used
- C1 and C2, combined with the amplifiers (A) implement the two integrators.
- CDACs are used to implement the DAC.



Implementation
Switched-Cap Filter: Response



- Frequency domain response of a 1st order and a 2nd order SDM.

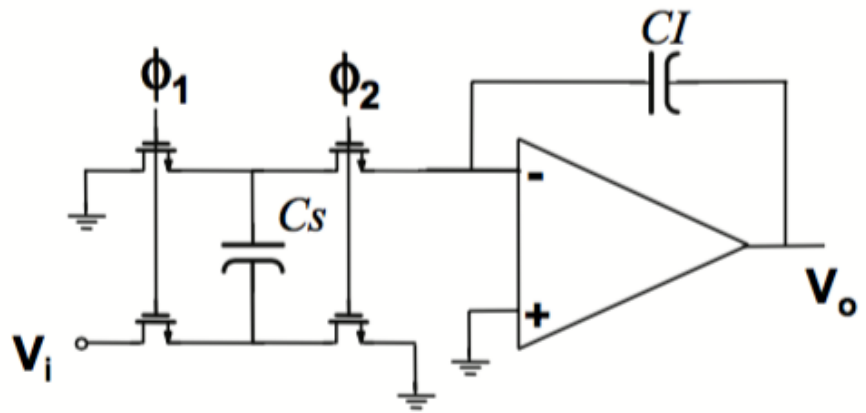
Non-Ideal Effects

Non Idealities

- Circuit non-idealities degrade performance of the SD ADC.
- Examples are:
  - Bandwidth limitation
  - Slew rate
  - Circuit noise

Non Idealities
Samping Noise

- Sampling noise power of a switched-capacitor circuit is proportional to kT/C.
- Due to oversampling, the effective sampling noise will be M = OSR times smaller than kT/C, i.e.: kT/MC.



$$\overline{v_n^2} = \frac{2KT}{Cs}$$

$$\overline{v_n^2}/f = 2\frac{kT}{Cs} \times \frac{1}{fs/2} = 4\frac{kT}{Cs \times fs}$$

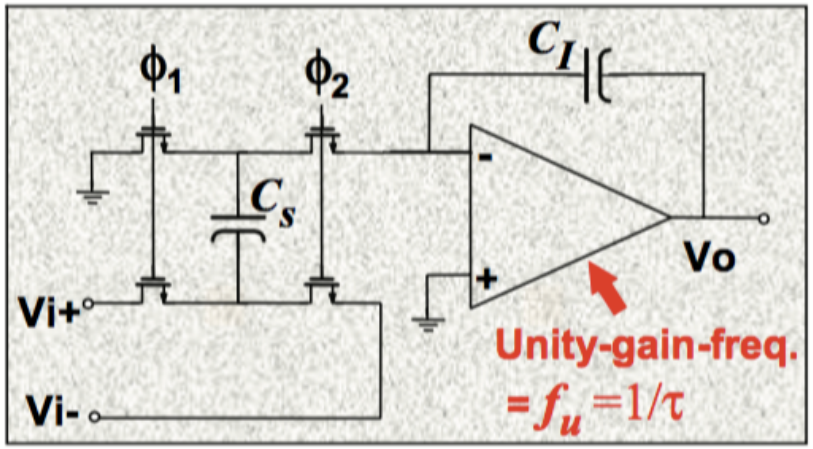
Total in-band noise:

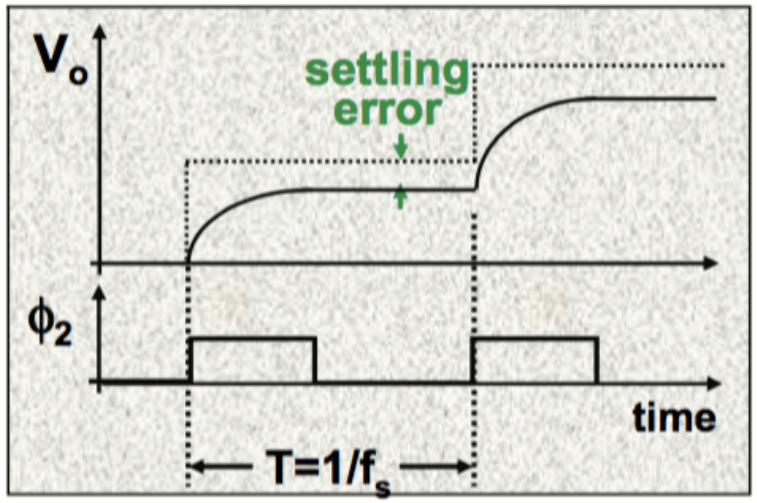
$$\overline{v_n^2}_{\ input-referred} = 4\frac{kT}{Cs \times fs} \times f_B$$

$$= \frac{2kT}{Cs \times M}$$

Non Idealities
Bandwidth

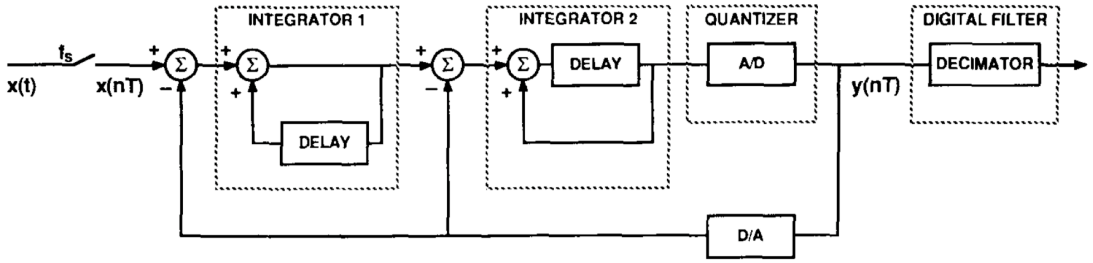
- In switched-cap circuits, generally, the GBW of amplifiers need to be at least 5x more than the switching frequency.
- In SDM systems, the amplifier GBW generally needs to be only two times more than the sampling clock frequency.
  - This is mainly because of noise and error shaping of the SDM loop.

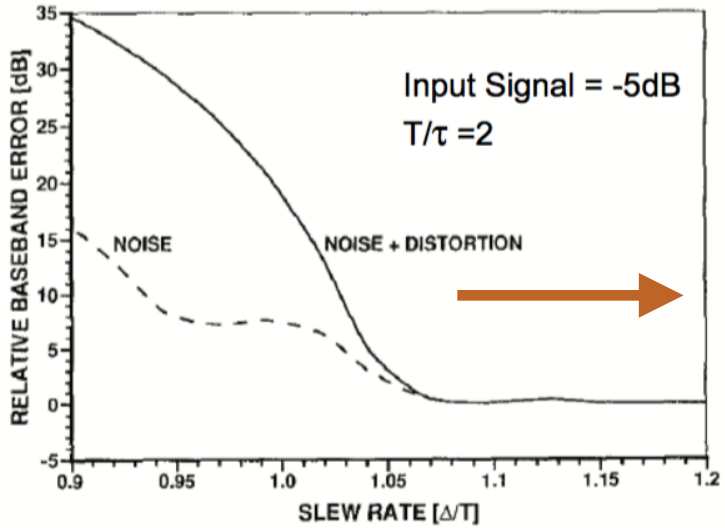




Non Idealities
Slew Rate

- Slew rate of amplifier adds some more error to the system.
- Example: in a 2nd order SDM, the amplifier SR (slew rate) needs to be 10% more than quantization noise, times the sampling frequency.

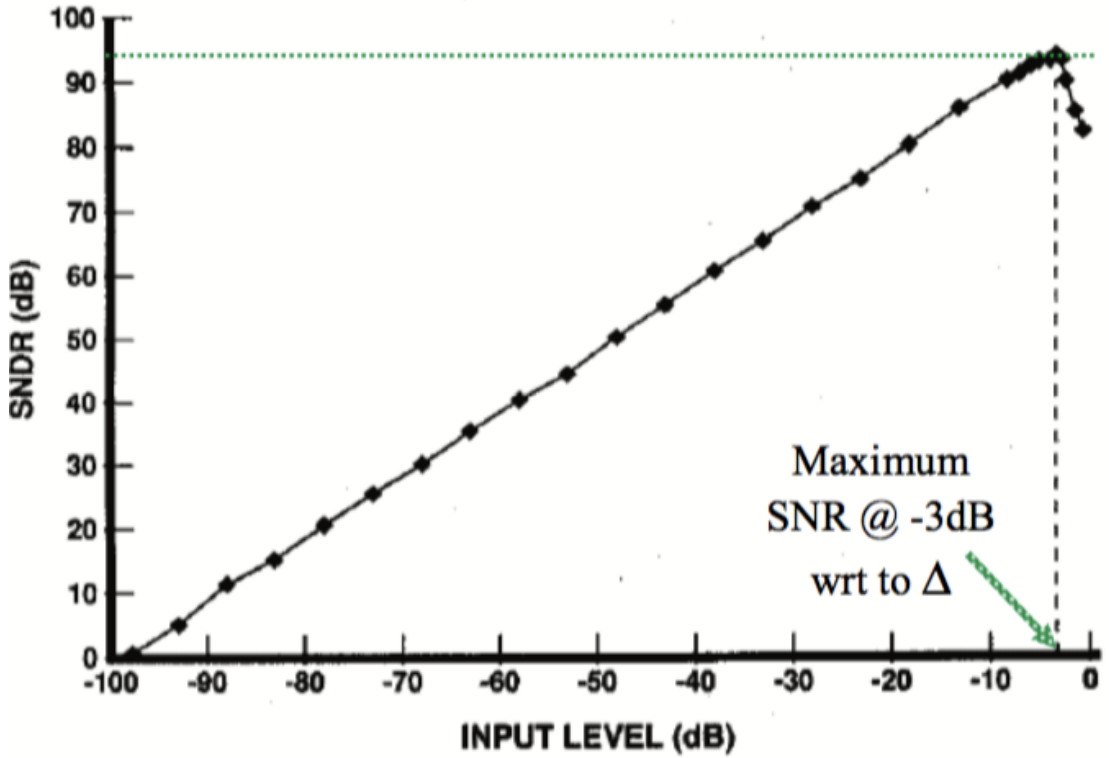




[Boser/Wooely, 1988]

Non Idealities
Voltage Swing

- The input full range for a SDM circuit is generally limited.
- For example, a 0dB input will cause saturation and even instability.
- The acceptable input full range is generally 3dB lower than the reference voltage level.



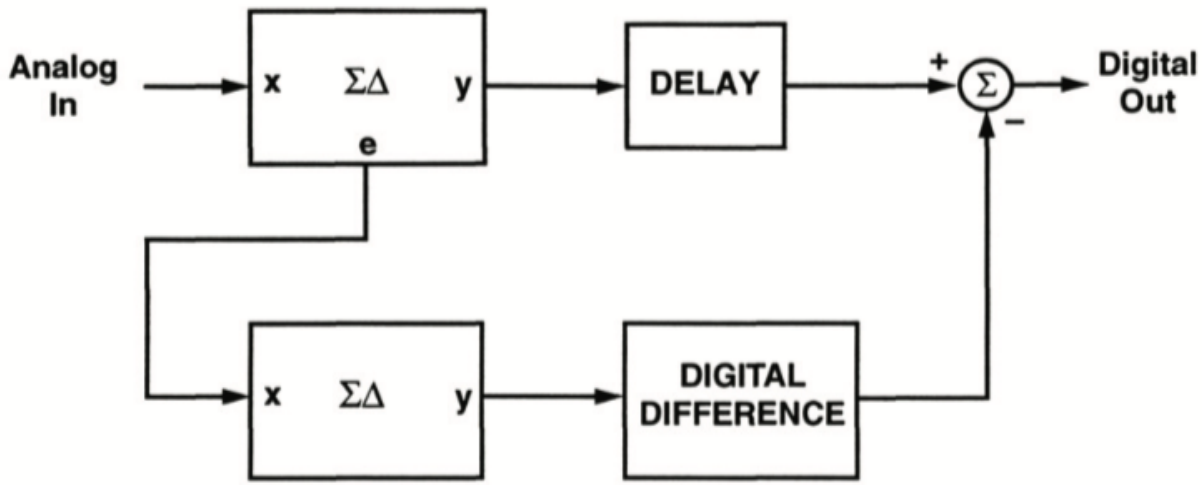
More Complex Topologies

Cascade and Mesh Topologies

Cascade Architecture

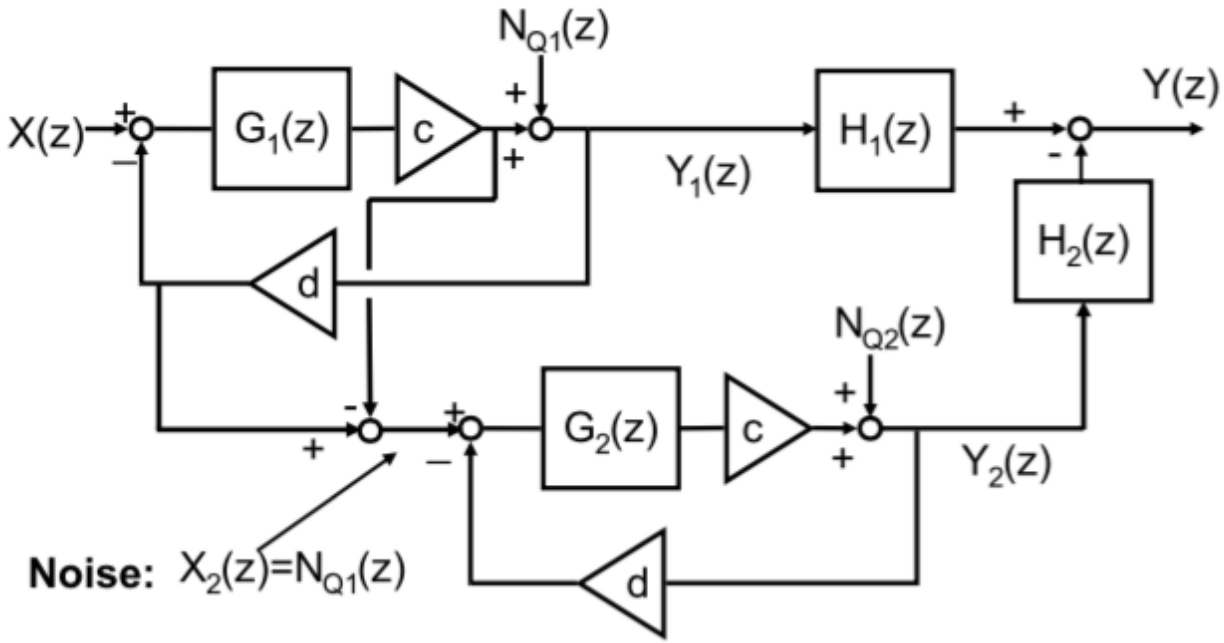
- Generally, it is very difficult to stabilities higher order modulators (n > 3)
- In order to further suppress the low-frequency quantization noise is to use cascade topologies.

- Example: 1-1 cascade structure.



Cascade Architecture

- Detailed block diagram of a 1-1 cascade architecture.



Cascade Architecture Analysis

$$Y_1(z) = \frac{G_1(z)}{1+G_1(z)}X(z) + \frac{1}{1+G_1(z)}N_{Q1}(z)$$

$$Y_2(z) = \frac{G_2(z)}{1+G_2(z)}N_{Q1}(z) + \frac{1}{1+G_2(z)}N_{Q2}(z)$$

$$Y(z) = \frac{H_1(z)G_1(z)}{1+G_1(z)}X(z) + \left(\frac{H_1(z)}{1+G_1(z)} - \frac{H_2(z)G_2(z)}{1+G_2(z)}\right)N_{Q1}(z) - \frac{H_2(z)}{1+G_2(z)}N_{Q2}(z)$$

Step 1:
Find the system transfer function

$$H_2(z)G_1(z) = H_1(z) = z^{-k}$$

Step 2:
STF should be all pass (with some delay)

$$Y(z) = X(z) + \frac{1}{G_1(z)G_2(z)}N_{Q2}(z)$$

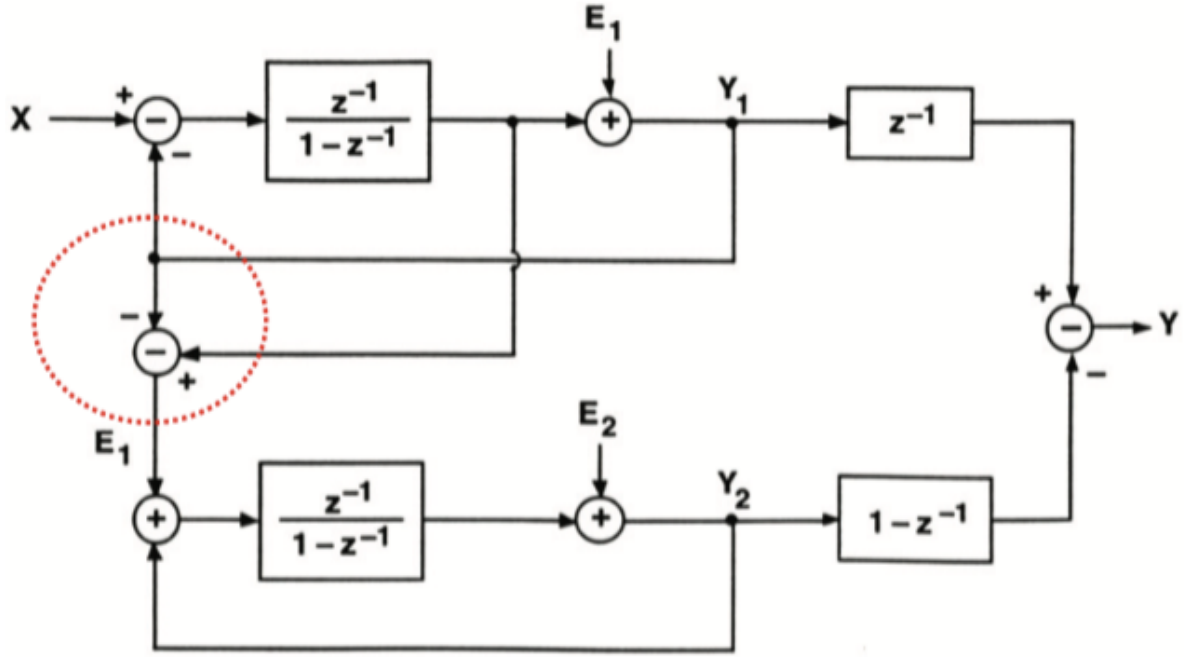
Step 3:
NTF should be high-pass

Cascade Architecture Example 1-1

$$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})E_1(z)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})Y_2(z)$$



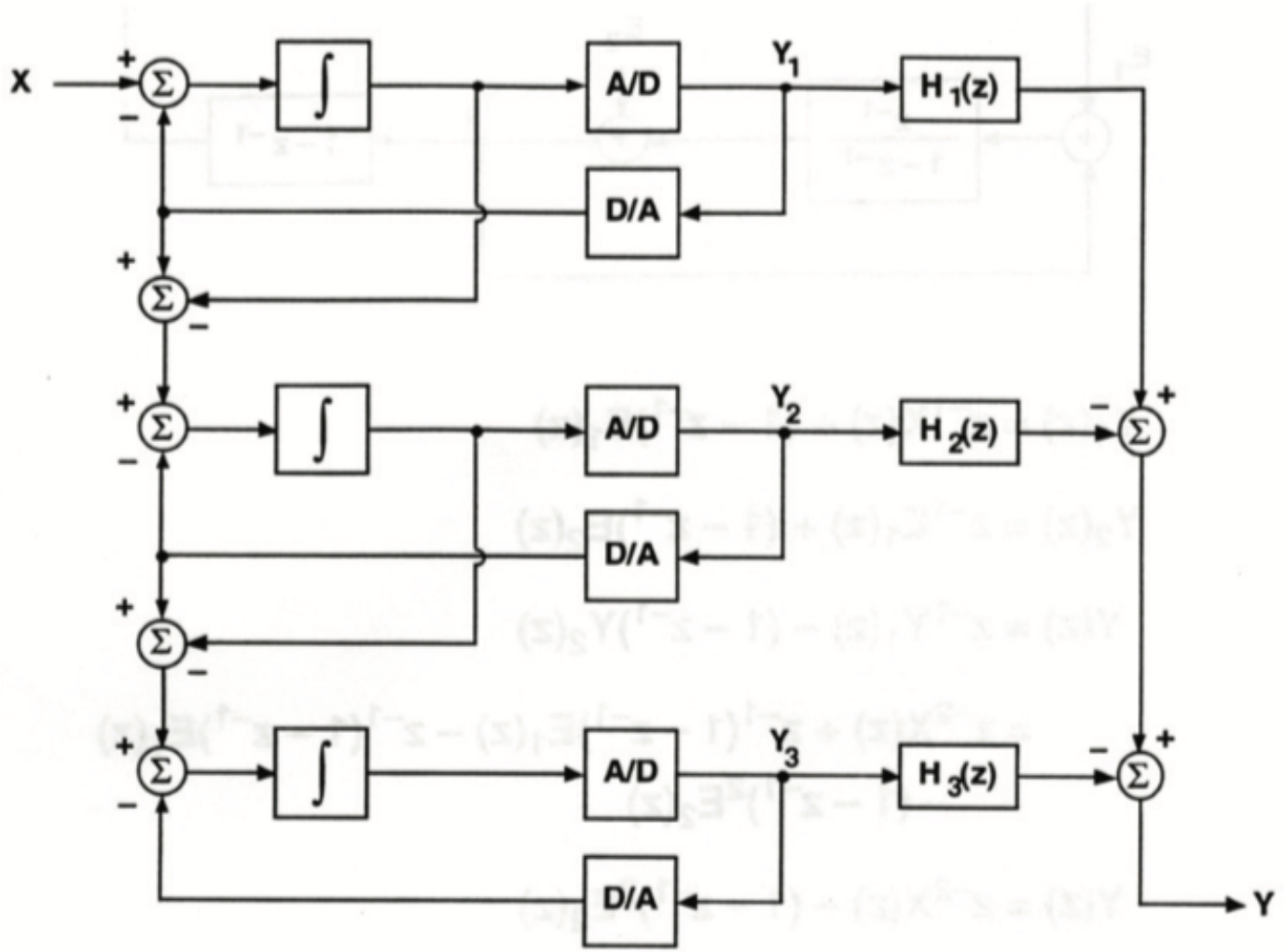
$$= z^{-2}X(z) + z^{-1}(1 - z^{-1})E_1(z) - z^{-1}(1 - z^{-1})E_1(z) - (1 - z^{-1})^2E_2(z)$$

$$\boxed{Y(z) = z^{-2}X(z) - (1 - z^{-1})^2E_2(z)}$$

2^{nd} order noise shaping

Cascade Architecture
Cascade 1-1-1

- Example: cascade 1-1-1
- STF/NTF: third order (60 dB/dec)



Cascade Architecture
Cascade 2-1

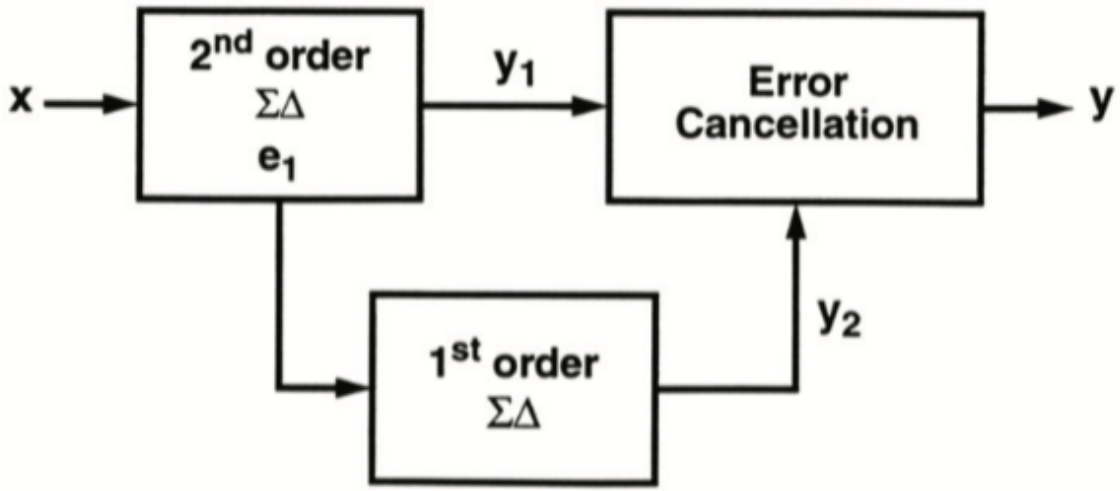
$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_1(z)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})^2 Y_2(z)$$

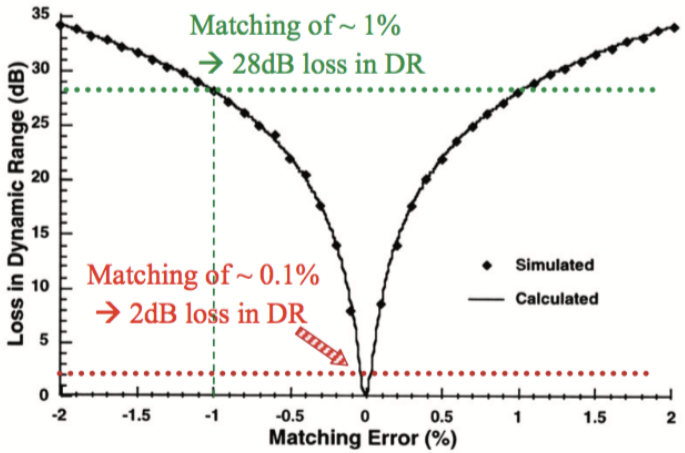
$$= z^{-3}X(z) + z^{-1}(1 - z^{-1})^2 E_1(z) - z^{-1}(1 - z^{-1})^2 E_1(z) - (1 - z^{-1})^3 E_2(z)$$

$$\boxed{Y(z) = z^{-3}X(z) - (1 - z^{-1})^3 E_2(z)}$$

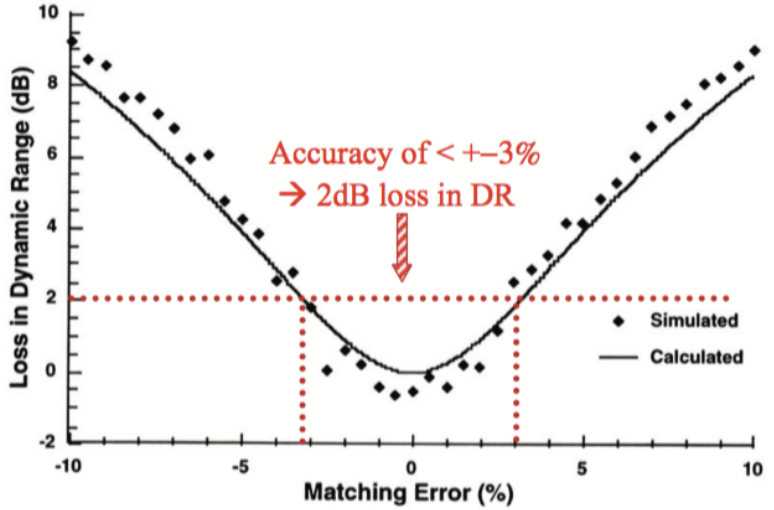


Cascade Architecture Robustness

Sensitivity of Cascade of (1-1-1) ΣΔ Modulators to Matching of Analog & Digital Paths

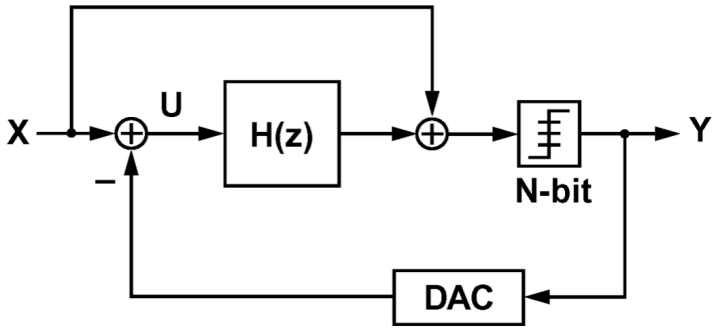


Sensitivity of Cascade of (2-1) ΣΔ Modulators to Matching Error



High Resolution ADC/DAC

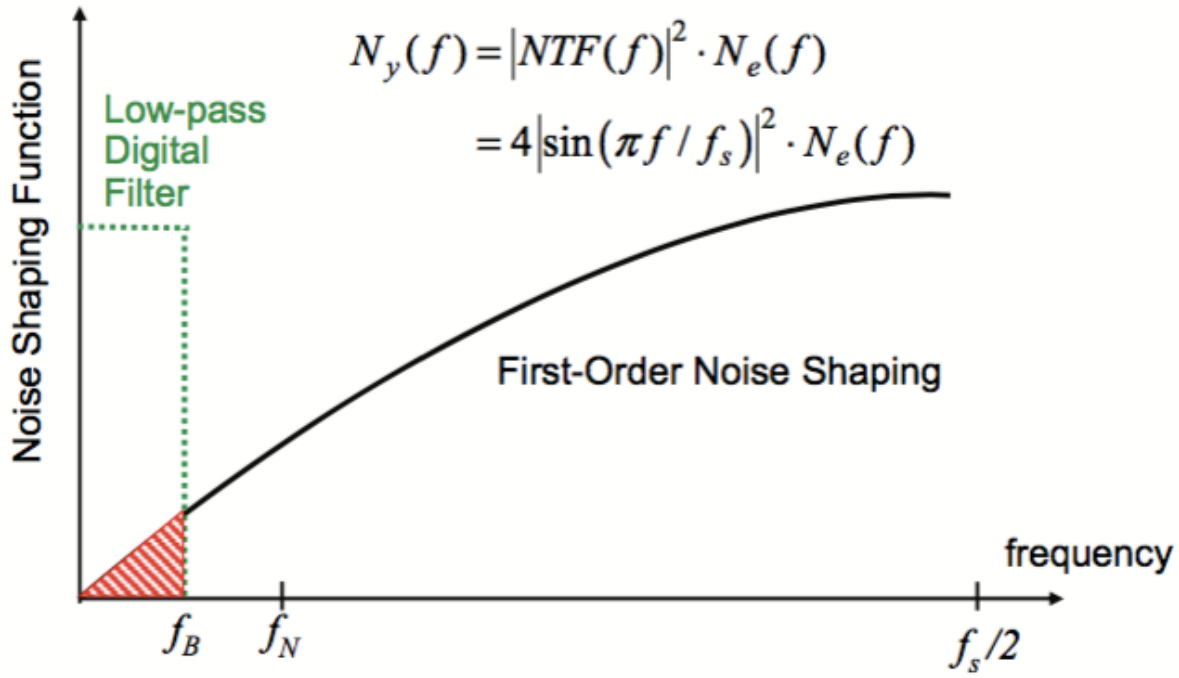
- The other possibility to increase the overall SDM resolution is to employ loop ADC/DAC with more than 1b resolution.



Resolution	ΔSNR
1 → 2	7.0 dB
2 → 3	6.2 dB
3 → 4	6.1 dB
4 → 5, etc.	6.0 dB

Decimation Filter

- How the noise bandwidth can be limited ?
- If no limitation, then noise should be integrated from DC to half the sampling frequency
- Solution: use digital low-pass filter
- In addition to rejecting the high frequency noise, the digital filter will reduce the rate of data (decimation filter)



Summary

Summary

- SD architecture is based on noise shaping and oversampling.
- SD ADCs are very popular in applications such as audio systems, wireless transceivers, and sensor interface.
- The energy-efficiency of SD ADCs is not as good as SAR architecture, however they offer much higher resolution.
- There are continuous-time and discrete-time SD implementations, the former is mostly being used in wireless applications, where speed is important, while the latter is used in sensor interfaces and audio.
- Mesh and cascade SD architectures can be utilized to enhance the resolution of the ADC.

References

References

[1] B. Boser, and Bruce A. Wooley, “The design of sigma-delta modulation analog-to-digital converters,” IEEE JSSC, 1988.

[2] B. P. Brandt, B. A. Wooley, “A 50-MHz multibit sigma-delta modulator for 12-b 2-MHz A/D conversion,” IEEE JSSC 1991.

[3] A. Tabatabaei, B. A. Wooley, “A two-path bandpass sigma-delta modulator with extended noise shaping,” IEEE JSSC 2002.

[4] R. Schreiner and G. C. Temes, Undrstanding deta-sigma data converters, Wiley 2005.